THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):

Harinath B. Kamepalli, Padmaraj Sanjeevarao, Chang-Jin Park

Assignee:

Sun Microsystems, Inc.

Title:

Scan Chain Verification Using Symbolic Simulation

Serial No.:

10/790,650

Filed:

March 1, 2004

Examiner:

Unknown

Group Art Unit:

Unknown

Docket No.:

SUN040292

Customer No.:

33438

Austin, Texas April 28, 2004

COMMISSIONER FOR PATENTS PO Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants wish to call the following documents to the attention of the Examiner.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

- 1. an admission that the documents are necessarily prior art with respect to the instant invention;
- 2. a representation that a search has been made, other than as described above; or
- 3._e an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, PO Box 1450, Alexandria, VA 22313-1450, on April 28, 2004.

Attorney for Applicant(s)

Data of Signature

Respectfully submitted,

Michael Rocco Cannatti Attorney for Applicant(s)

Reg. No. 34,791

U.S. Department of Commerce, Patent and Trademark Office					Attorne	Attorney Docket No.		Serial No.		
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INFORMATION DISCLOSURE STATEMENT BY APPLICATED					Applica	Applicant(s)				
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*Examiner		Document					Filing Date If Appropriate			
Initial	AA	Number 6,634,012	Date 10/14/2003	Name Zhong et al.	Class 716	Subclass 5	If Appro	priate		
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	AR Takahashi, Tsuyoshi, et al., "Design Flow and Design Environment for System LSIs," Hitachi Review Vol. 48 (1999) No. 2, pp. 87-93									
	AS	Kurup, Pran, et al., "Mastering HDL for formal verification," Electronics Engineer, May 1999								
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Sheet 2 of 3

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)										
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	AS	http://www.synopsys.com/products/acmgr/innlo/espcv.html, "ESP-CV"								
	AT	http://www.synopsys.com/products/acmgr/innlo/esplv.html, "ESP-LV"								
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.										

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U.S. Department of Commerce, Patent and Trademark Office					Attorne	Attorney Docket No.		Serial No.	
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	AS	http://www.synopsys.com/products/acmgr/innlo/ckt.html, "CKT"							
	AT	http://www.synopsys.com/products/acmgr/innlo/casestudy/suncase.html, "Case Study"							
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